WHAT IS CLAIMED IS:

1. A microprocessor including:

a program control unit controlling fetch of an instruction code;

an instruction decode unit decoding said fetched instruction code;

an address operation unit operating an address of a memory on the basis of the result of decoding by said instruction decode unit; and

a data operation unit operating data on the basis of the result of decoding by said instruction decode unit, wherein

said data operation unit executes data transfer between registers and data transfer between said registers and said memory in correspondence to single said instruction code having a single operation code fetched by said program control unit.

2. The microprocessor according to claim 1, wherein said data operation unit transfers data stored in a first register to said memory and transfers data stored in a second register to said first register in correspondence to a single push instruction fetched by said program control unit.

3. The microprocessor according to claim 2, wherein said data operation unit decrements the value of a stack pointer after transferring said data stored in said second register to said first register.

4. The microprocessor according to claim 2, wherein said first register is a work register implemented in said data operation unit.

5. The microprocessor according to claim 2, wherein said second register is a control register implemented in one of said address operation unit and said program control unit.

6. The microprocessor according to claim 1, wherein said data operation unit transfers data stored in a first register to a second register

and transfers data stored in said memory to said first register in correspondence to a single pop instruction fetched by said program control unit.

7. The microprocessor according to claim 6, wherein said data operation unit increments the value of a stack pointer after transferring said data stored in said memory to said first register.

8. The microprocessor according to claim 6, wherein said first register is a work register implemented in said data operation unit.

9. The microprocessor according to claim 6, wherein said second register is a control register implemented in one of said address operation unit and said program control unit.

10. The microprocessor according to claim 1, wherein said data operation unit transfers data stored in a first register to said memory and keeps the value of a stack pointer unchanged for a single push instruction fetched by said program control unit.

11. An assembler including:

a code reading unit reading a code from a source program;

a storage unit storing information for specifying a plurality of registers;

a first code generation unit storing said information for specifying said plurality of registers included in said code read by said code reading unit in said storage unit and generating a code to push data stored in said plurality of registers when said code is a first macro instruction; and

a second code generation unit referring to said information for specifying said plurality of registers stored in said storage unit and generating a code to pop data stored in said plurality of registers when said code read by said code reading unit is a second macro instruction.

12. The assembler according to claim 11, wherein said first code generation unit generates a code to push data stored in registers other than a register used as a medium for data transfer between said registers and a memory among said plurality of registers included in said code when said code read by said code reading unit is said first macro instruction.

13. A storage medium, readable by a computer, on which an assembly program for making said computer execute an assembly method is recorded, said assembly method comprising the steps of:

reading a code from a source program;

storing information for specifying a plurality of registers included in said code and generating a code to push data stored in said plurality of registers when said code is a first macro instruction; and

referring to said stored information for specifying said plurality of registers and generating a code to pop data stored in said plurality of registers when said read code is a second macro instruction.

14. The recording medium recording an assembly program according to claim 13, wherein said step of storing information for specifying a plurality of registers included in said code and generating said code to push data stored in said plurality of registers includes the step of generating a code to push data stored in registers other than a register used as a medium for data transfer between said registers and a memory among said plurality of registers included in said read code when said read code is said first macro instruction.